WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, comprising:

defining a region where a ferroelectric capacitor is formed by using a mask for forming and processing any one of a lower electrode layer and an upper electrode supporting layer prior to forming an upper electrode layer;

wherein the lower electrode layer extending in a first direction and the upper electrode layer extending in a second direction are provided on a semiconductor substrate with a ferroelectric layer and the upper electrode supporting layer therebetween, and the ferroelectric capacitor is provided at an intersection of the lower electrode layer and the upper electrode layer.

2. The method for manufacturing a semiconductor device according to Claim 1, wherein a dimension in the first direction of the region where the ferroelectric capacitor is formed is larger than the width of the upper electrode layer.

3. The method for manufacturing a semiconductor device according to Claim 1, wherein a dimension in the second direction of the region where the ferroelectric capacitor is formed is larger than the width of the lower electrode layer.

4. A method for manufacturing a semiconductor device, comprising:

depositing a lower electrode layer forming film, a ferroelectric layer forming film, and an upper electrode supporting layer forming film in this order on a semiconductor substrate;

depositing an upper electrode supporting layer forming mask on the upper electrode supporting layer forming film;

forming an upper electrode supporting layer in a region where a ferroelectric capacitor is formed by using the upper electrode supporting layer forming mask;

depositing a lower electrode layer forming mask on the ferroelectric layer forming film in the presence of the upper electrode supporting layer forming mask;

forming a ferroelectric layer and a lower electrode layer in the region where the ferroelectric capacitor is formed and in a region where the lower electrode layer is formed extending in a first direction including the region where the ferroelectric capacitor is formed, respectively, by using the upper electrode supporting layer forming mask and the lower electrode layer forming mask;

forming an insulating layer on the whole upper surface of the semiconductor substrate from which the upper electrode supporting layer forming mask and the lower electrode layer forming mask have been removed;

exposing an upper surface of the upper electrode supporting layer that is to be the region where the ferroelectric capacitor is formed to an upper surface of the insulating layer; and

forming an upper electrode layer extending in a second direction on the insulating layer to which the upper surface of the upper electrode supporting layer has been exposed so as to include the region where the ferroelectric capacitor is formed;

wherein the lower electrode layer extending in the first direction and the upper electrode layer extending in the second direction are provided on the semiconductor substrate with the ferroelectric layer and the upper electrode supporting layer therebetween, and the ferroelectric capacitor is provided at an intersection of the lower electrode layer and the upper electrode layer.

5. The method for manufacturing a semiconductor device according to Claim 4, wherein the upper electrode supporting layer forming mask is made of a material having an etching resistance higher than an etching resistance of the lower electrode layer forming mask.

6. The method for manufacturing a semiconductor device according to Claim 4, wherein the lower electrode layer forming mask is made of a material having an etching resistance higher than an etching resistance of the upper electrode supporting layer forming mask.

7. The method for manufacturing a semiconductor device according to Claim 4, wherein the upper electrode supporting layer is made larger than an area to be occupied by an intersection of the upper electrode layer and the lower electrode layer by using the upper electrode supporting layer forming mask.

8. A semiconductor device, comprising:

a ferroelectric capacitor formed in a region larger than an area occupied by an intersection of a lower electrode layer and an upper electrode layer;

wherein the lower electrode layer extending in a first direction and the upper electrode layer extending in a second direction are provided on a semiconductor substrate with a ferroelectric layer and an upper electrode supporting layer therebetween, and the ferroelectric capacitor is provided at the intersection of the lower electrode layer and the upper electrode layer.

9. The semiconductor device according to Claim 8, wherein a dimension in the first direction of the region where the ferroelectric capacitor is formed is larger than the width of the upper electrode layer.

10. The semiconductor device according to Claim 8, wherein a dimension in the second direction of the region where the ferroelectric capacitor is formed is larger than the width of the lower electrode layer.